Accurate and Efficient Circuit Simulation with Lumped-Element FDTD Technique

Paolo Ciampolini, Paolo Mezzanotte, *Member, IEEE,*
Luca Roselli, *Member, IEEE,* and Roberto Sorrentino, *Fellow, IEEE*

***Abstract*— A three-dimensional (3-D) implementation of the lumped-element finite-difference time-domain (FDTD) algorithm has been carried out. To accomplish proper description of device dynamic responses, the code incorporates accurate models of lumped bipolar devices, including nonlinear capacitances associated with pn and Schottky junctions. The nonlinear system arising from discretized lumped-element equations is solved by means of an iterative Newton–Raphson algorithm, the convergence properties of which are sensitive to the value of the simulation time step. The computational efficiency of the algorithm (as well as its robustness) has significantly been enhanced by introducing an adaptive time-step algorithm, which dynamically adjusts the time-step itself to ensure convergence during the simulation. Several simulation examples are compared with conventional analysis techniques and demonstrate the algorithm reliability as well as its increased efficiency.**

I. Introduction

OVER LAST two decades circuit simulation tools (and, primarily, SPICE [1]) have had a substantial impact on circuit design methodology. Such tools constitute the heart of modern CAD systems, and a huge amount of work has been devoted to formulate compact, yet complete, models of active devices of any kind. Within most CAD frameworks, however, much lesser attention has been paid to the behavior of the passive part of the circuit; transmission lines are customarily described by lumped-element equivalent circuits, and whenever the propagation of electromagnetic signals plays a dominant role, such an approximation may result in large inaccuracies. Furthermore, the equivalent-circuit approach can hardly take into account phenomena such as crosstalk, radiative, or packaging effects; the inherently distributed nature of these effects calls indeed for a more physical description.

Basically, a "full-wave" solution of Maxwell's equations can provide a deeper insight into the passive network behavior. Among suitable numerical techniques, the finite-difference time-domain (FDTD) method has been established as a versatile and computationally effective approach. Such an algorithm, first presented by Yee in 1966 [2], has been successfully applied to the analysis of different problems, ranging from electromagnetic scattering [3] to wave propagation [4] and biocompatibility issues [5]. More recently, Sui *et al.* [6] worked out an extended formulation of the FDTD algorithm that introduces external lumped elements. Within this approach, the constitutive relationships of lumped devices are assumed as boundary conditions for the FDTD equations, without requiring heavy modifications of the original scheme. A three-dimensional (3-D) extension of Sui's algorithm was reported later by May *et al.* [7]. The same approach was applied by Thomas *et al.* [8] to the simulation of an active antenna, including a Gunn diode. In principle, distributed device models can be incorporated into the solution of Maxwell's equations as well. This technique, although feasible [9], demands large computational resources, and is therefore not suitable for the simulation of complex circuits. The lumped assumption actually holds as long as the device active region is small compared with the signal shortest wavelength, so that the device can be treated as zero dimensional, with respect to wave propagation. For most devices, such an assumption is largely justified up to frequencies of several tens of THz and is therefore appropriate for the simulation of most circuits of practical interest. In this paper, the same approach of [6] and [7] is followed for the purpose of turning a FDTD Maxwell's equation solver into an efficient and reliable tool for circuit analysis. Within this context, however, some algorithmic complexities need to be tackled, mostly connected to the behavior of nonlinear lumped devices.

In the cited works, in fact, only basic device models have been considered. Most notably, junction dynamic effects have often been neglected, this limiting the validity range of such models to narrow-frequency bands. Some classes of circuits cannot therefore be reliably described by such an approach. In the following, we describe the inclusion of a more general set of models into our 3-D FDTD code. More specifically, the conventional, low-frequency models of pn and Schottky junctions have been supplemented with the equations accounting for the nonlinear intrinsic capacitances associated with the junctions themselves. The discrete formulation of such models is introduced in Section II below. Section III, in turn, deals with numerical issues related to the inclusion of nonlinear lumped elements. Regardless of the model adopted, in fact, this requires to solve a system of nonlinear equations at each simulation time step. To this purpose, iterative procedures such as the Newton-Raphson (NR) algorithm can be employed. An undesirable degree of uncertainty is, however, introduced in the (otherwise deterministic) FDTD algorithm. Under some circumstances, the NR scheme may indeed diverge, causing the simulation to abort.

In order to ensure the convergence of the procedure, it is often necessary to reduce the simulation time step, even far below the upper limit imposed by the Courant stability criterion (i.e., the time step required by the simulation of the passive network alone). This need mostly arises as the signals undergo abrupt changes, so that more stringent requirements

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The authors are with the Istituto di Elettronica, Università di Perugia, Via G. Duranti 1/A-1, I-06131, Perugia, Italy.

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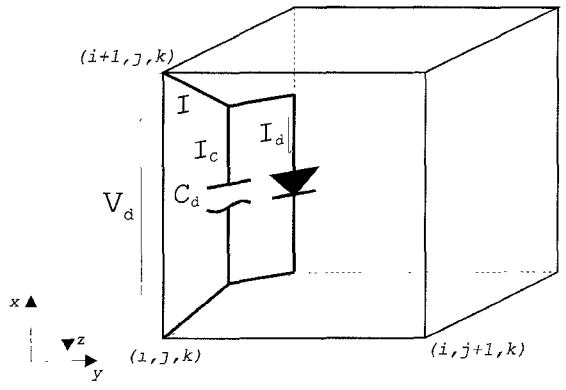


Fig. 1. Equivalent circuit of the diode.

are likely to come only from short periods within the simulation timeframe. In the usual framework a constant time step is adopted, just like in the plain FDTD scheme. In this case, the time step has to be settled by a worst-case prediction. The adoption of such a conservative estimate, however, may significantly slow down the entire simulation. To overcome this problem, a variable time-step scheme has been devised and implemented in which the time step itself is adaptively chosen by monitoring the convergence rate of the nonlinear solution.

Some application examples are shown in Section IV; in particular, a simple clamping-diode circuit has been simulated to illustrate basic method features, whereas a more realistic example is given by the analysis of a simple unbalanced mixer with a filtering stub. Finally, a more complex circuit has been simulated that consists of a microstrip connection between two high-speed logic gates; due to the steep edges of digital signals, this example represents a significant testbed for evaluating the computational performance of the proposed time-adaptive algorithm.

II. The Lumped-Element FDTD Algorithm

To account for lumped elements, we start from Maxwell curl equation

$$\operatorname{curl}(\overline{H}) = \varepsilon \frac{d\overline{E}}{dt} + \overline{J}_c. \tag{1}$$

The conduction current density $\overline{J}_c$ in the above equation can be split into two separate contributions

$$\overline{J}_c = \overline{J}_{cd} + \overline{J}_{cl}. \tag{2}$$

Here, $\overline{J}_{cd}$ represents the contribution of the current density flowing along the distributed media (expressed in the customary way within the FDTD scheme), whereas $\overline{J}_{cl}$ stands for the contribution of the lumped elements. Linear, as well as nonlinear, lumped elements may show up in the latter term. Resistors, capacitors, inductors, and voltage sources are modeled according to the literature [7]. Unlike [7], however, the current flowing across a pn-junction is expressed as follows:

$$\begin{aligned} I &= I_d + I_c = I_d + \frac{dQ_d}{dt} \\ &= I_0(e^{q(V_d/\eta\cdot k\cdot T)} - 1) + C_d(V_d)\frac{dV_d}{dt}. \end{aligned} \tag{3}$$

Where V_d is the diode applied voltage, I_0 is the inverse saturation current, η is the junction emission coefficient, and $C_d(V_d)$ represents the capacitance associated with the junction. More specifically, such a capacitance can be ascribed to two concurrent effects: 1) the width modulation of the junction space-charge region and; 2) the injection of minority carriers across the junction. Consequently, two terms [10], [11] are considered

$$C_d(V_d) = C_j(V_d) + C_D(V_d). \tag{4}$$

C_j accounts for the first effect above and is more properly termed "junction capacitance." A regional approximation is assumed in order to model such a contribution, depending on the bias regime of the junction

$$C_J(V_d) = C_J(0) \cdot \left(1 - \frac{V_d}{\Phi_0}\right)^{-m} \quad \text{if} \quad V_d < F_c \cdot \Phi_0 \tag{5a}$$

$$C_J(V_d) = \frac{C_J(0)}{F_2} \cdot \left(F_3 + \frac{m \cdot V_d}{\Phi_0}\right) \quad \text{if} \quad V_d \geq F_c \cdot \Phi_0. \tag{5b}$$

In (5), m is a coefficient related to the doping profile ($m = 0.5$ for abrupt junctions), Φ_0 is the junction built-in voltage, $C_J(0)$ is the zero-bias junction capacitance, and F_c, F_2, F_3 are suitable constants. In particular, the forward-bias capacitance in (5b) is obtained by a linear extrapolation of (5a), which holds within the reverse bias region. In forward-bias regimes, however, the dynamic behavior of the junction is largely dominated by the diffusion capacitance

$$C_D = \frac{q}{\eta \cdot K \cdot T} \tau_D I_0 e^{(q/\eta\cdot K\cdot T)\cdot V_d} \tag{6}$$

in which τ_D depends on the carrier lifetimes [10]. Schottky diodes can be modeled in the same way, except for the absence of the diffusion capacitance.

The current density $\overline{J}_{cl}$, to be incorporated into (1), can be evaluated by (3)–(6). The discretization of $\overline{J}_{cl}$ can then be carried out assuming the standard Yee's notation, and following the same guidelines as in [6], [7]. With reference to Fig. 1, the x-component of $\overline{J}_{cl}$ reads as follows:

$V_D \geq -F_c \cdot \Phi_0$:

$$\begin{aligned} &J_{clx}^{n+(1/2)}\left(i+\frac{1}{2}, j, k\right) \\ &= -\frac{I_0}{\Delta y \cdot \Delta z} \cdot \left(\exp\left[-\frac{q}{\eta \cdot K \cdot T} \cdot \Delta x \right.\right. \\ &\quad \left.\left. \cdot \frac{E_x^{n+1}(i+\frac{1}{2}, j, k) + E_x^n(i+\frac{1}{2}, j, k)}{2}\right] - 1\right) \\ &\quad + \frac{1}{\Delta y \cdot \Delta z} \cdot \left\{\tau_D \cdot I_0 \cdot \frac{q}{\eta \cdot K \cdot T} \right. \\ &\quad \cdot \exp\left[-\frac{q}{\eta \cdot K \cdot T} \cdot \Delta x \right. \\ &\quad \left.\left. \cdot \frac{E_x^{n+1}(i+\frac{1}{2}, j, k) + E_x^n(i+\frac{1}{2}, j, k)}{2}\right] \right. \\ &\quad + C_J(0) \cdot \left[1 + \frac{\Delta x}{\Phi_0} \right. \\ &\quad \left.\left. \cdot \frac{(E_x^{n+1}(i+\frac{1}{2}, j, k) + E_x^n(i+\frac{1}{2}, j, k))}{2}\right]^{-m}\right\} \\ &\quad \cdot \Delta x \cdot \frac{E_x^{n+1}(i+\frac{1}{2}, j, k) - E_x^n(i+\frac{1}{2}, j, k)}{\Delta t} \end{aligned} \tag{7a}$$

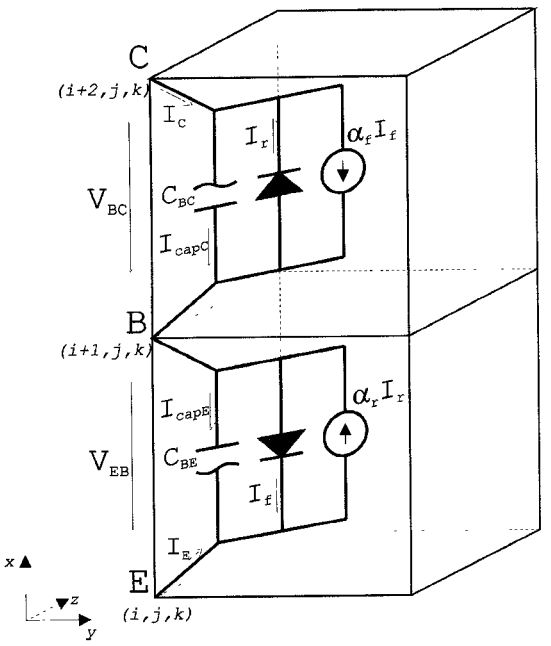


Fig. 2. Equivalent circuit of the bipolar transistor.

$V_D < F_c \cdot \Phi_0$:

$$
\begin{aligned}
&J_{clx}^{n+(1/2)}\left(i+\frac{1}{2},j,k\right)\\
&\quad=-\frac{I_0}{\Delta y\cdot\Delta z}\cdot\left(\exp\left[-\frac{q}{\eta\cdot K\cdot T}\cdot\Delta x\right.\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{1}{2},j,k)+E_x^{n}(i+\frac{1}{2},j,k)}{2}\right]-1\right)\\
&\qquad+\frac{1}{\Delta y\cdot\Delta z}\cdot\left\{\tau_D\cdot I_0\cdot\frac{q}{\eta\cdot K\cdot T}\cdot\exp\left[-\frac{q}{\eta\cdot K\cdot T}\right.\right.\\
&\qquad\left.\cdot\Delta x\cdot\frac{E^{n+1}x(i+\frac{1}{2},j,k)+E_x^{n}(i+\frac{1}{2},j,k)}{2}\right]\\
&\qquad+\frac{C_J(0)}{F_2}\cdot\left[F_3-\frac{m\cdot\Delta x}{\Phi_0}\right.\\
&\qquad\left.\left.\cdot\frac{(E_x^{n+1}(i+\frac{1}{2},j,k)+E_x^{n}(i+\frac{1}{2},j,k))}{2}\right]\right\}\\
&\qquad\cdot\Delta x\cdot\frac{E_x^{n+1}(i+\frac{1}{2},j,k)-E_x^{n}(i+\frac{1}{2},j,k)}{\Delta t}. \qquad (7b)
\end{aligned}
$$

Time derivatives in (7) are actually averaged between time-steps n and $n+1$, consistently with the treatment of the other terms in (1) [7]. After incorporation of (7), the discretized expression of (1) becomes strongly nonlinear, as detailed in Section III. This requires the adoption of suitable solution algorithms.

Bipolar transistors are taken into account by arranging a network of nonideal junction diodes and current-controlled current-sources [10], according to the scheme depicted in Fig. 2.

Referring to such an equivalent circuit, the transistor currents can be expressed as follows:

$$
\begin{aligned}
I_E &= \alpha_R I_R - I_F - I_{\mathrm{cap}E}\\
I_C &= I_R - \alpha_F I_F + I_{\mathrm{cap}C} \qquad (8)
\end{aligned}
$$

where

$$
\begin{aligned}
I_F &= I_{0F}(e^{qV_{BE}/\eta_F\cdot k\cdot T}-1)\\
I_R &= I_{0R}(e^{qV_{BC}/\eta_R\cdot k\cdot T}-1). \qquad (9)
\end{aligned}
$$

The discretization of the above equations follows the same strategy discussed above. For instance, let us assume the BJT is biased in the active-forward region, with the emitter located at cell (i,j,k) and the collector located at cell $(i+1,j,k)$. The following expressions of discretized emitter and collector current densities can be worked out:

$$
\begin{aligned}
&J_{clxC}^{n+(1/2)}\left(i+\frac{3}{2},j,k\right)\\
&\quad=\frac{I_{0R}}{\Delta y\cdot\Delta z}\cdot\left(\exp\left[\frac{q}{\eta_R\cdot K\cdot T_C}\cdot\Delta x\right.\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{3}{2},j,k)+E_x^{n}(i+\frac{3}{2},j,k)}{2}\right]-1\right)\\
&\qquad-\alpha_F\frac{I_{0F}}{\Delta y\cdot\Delta z}\cdot\left(\exp\left[-\frac{q}{\eta_F\cdot K\cdot T_E}\cdot\Delta x\right.\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{1}{2},j,k)+E_x^{n}(i+\frac{1}{2},j,k)}{2}\right]-1\right)\\
&\qquad+\frac{1}{\Delta y\cdot\Delta z}\cdot\left\{\tau_{DC}\cdot\alpha_R\cdot I_{0R}\cdot\frac{q}{\eta_R\cdot K\cdot T_C}\right.\\
&\qquad\cdot\left(\exp\left[\frac{q}{\eta_R\cdot K\cdot T_C}\cdot\Delta x\right.\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{3}{2},j,k)+E_x^{n}(i+\frac{3}{2},j,k)}{2}\right]-1\right)\\
&\qquad+C_{JC}(0)\cdot\left(1-\Delta x\right.\\
&\qquad\left.\left.\cdot\frac{(E_x^{n+1}(i+\frac{3}{2},j,k)+E_x^{n}(i+\frac{3}{2},j,k))}{2\Phi_{0C}}\right)^{-m_C}\right\}\\
&\qquad\cdot\Delta x\cdot\frac{E_x^{n+1}(i+\frac{3}{2},j,k)-E_x^{n}(i+\frac{3}{2},j,k)}{\Delta t} \qquad (10a)\\
&J_{clxE}^{n+(1/2)}\left(i+\frac{1}{2},j,k\right)\\
&\quad=\alpha_R\frac{I_{0R}}{\Delta y\cdot\Delta z}\left(\exp\left[\frac{q}{\eta_R\cdot K\cdot T_C}\cdot\Delta x\right.\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{3}{2},j,k)+E_x^{n}(i+\frac{3}{2},j,k)}{2}\right]-1\right)\\
&\qquad-\frac{I_{0F}}{\Delta y\cdot\Delta z}\left(\exp\left[-\frac{q}{\eta_F\cdot K\cdot T_E}\cdot\Delta x\right.\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{1}{2},j,k)+E_x^{n}(i+\frac{1}{2},j,k)}{2}\right]-1\right)\\
&\qquad+\frac{1}{\Delta y\cdot\Delta z}\left\{\tau_{DE}\cdot\alpha_F\cdot I_{0F}\cdot\frac{q}{\eta_F\cdot K\cdot T_E}\right.\\
&\qquad\cdot\exp\left[-\frac{q}{\eta_F\cdot K\cdot T_E}\cdot\Delta x\right.\\
&\qquad\left.\left.\cdot\frac{E_x^{n+1}(i+\frac{1}{2},j,k)+E_x^{n}(i+\frac{1}{2},j,k)}{2}\right]\right.\\
&\qquad+\frac{C_{JE}(0)}{F_{2E}}\left[F_{3E}-\frac{m_E\cdot\Delta x}{\Phi_{0E}}\right.
\end{aligned}
$$

TABLE I
ORIGINAL FDTD ALGORITHM [1]

1. For t from 0 to final time step
1.1. update H-field components
1.2. apply H-field boundary conditions
1.3. update E-field components
1.4. apply E-field boundary conditions

TABLE II
TIME-ADAPTIVE FDTD ALGORITHM

1. For t from 0 to final time
1.1. check for convergence of non-linear equations
1.2. if convergence
1.2.1. do until divergence
1.2.1.1. increase Δt
1.2.1.2. check for convergence
1.2.2. restore last "converging" Δt
1.3. else if divergence
1.3.1. do until convergence
1.3.1.1. decrease Δt
1.3.1.2. check for convergence
1.4. update H-field components
1.5. apply H-field boundary conditions
1.6. update E-field components
1.7. apply E-field boundary conditions

$$\cdot \frac{(E_x^{n+1}(1+\frac{1}{2},j,k)+E_x^{n}(1+\frac{1}{2},j,k))}{2}\Bigg]\Bigg\}$$
$$\cdot \Delta x \cdot \frac{E_x^{n+1}(1+\frac{1}{2},j,k)-E_x^{n}(1+\frac{1}{2},j,k)}{\Delta t}. \quad (10b)$$

Current densities (10a) and (10b) involve two unknowns [namely $E_x^{n+1}(i+1/2,j,k)$ and $E_x^{n+1}(i+3/2,j,k)$] in a coupled fashion. Hence, in this case, the solution of a system of two nonlinear equations is to be sought for.

Although the present discussion has been limited to bipolar devices, different kinds of devices can easily be accomplished. The large-signal equivalent circuits of other devices can be implemented by assembling along different patterns the same building blocks developed so far.

III. TIME ADAPTIVE SOLUTION TECHNIQUE

In the general case, lumped-element nonlinear equations cannot be given a closed-form solution; therefore, a successive approximation strategy must be followed, such as the well-known Newton-Raphson method. An exhaustive discussion of the NR algorithm is beyond the scope of this paper. Here, we will content ourselves with a short summary. Basically, the NR scheme relies on the iterative solution of the linearized system. In order to properly initialize such an iterative loop, a first guess solution must be given, the "quality" of which, in turn, strongly affects the convergence rate. Once the transient simulation is started, it is a common practice to assume, at each time step, the previous solution as the current first guess. Whenever a sudden change of the signals occurs, however, initial guess provided by this technique may fall

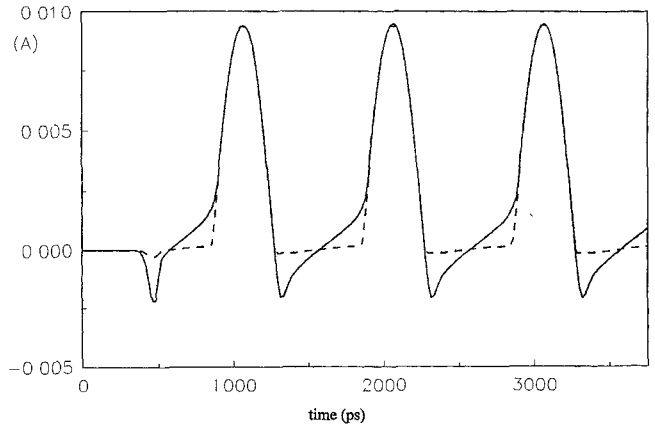


Fig. 3. FDTD simulation of the diode-terminated microstrip connection: computed diode current (input voltage-source frequency: 1 GHz). Dashed line: without capacitances; solid line: with nonlinear capacitances.

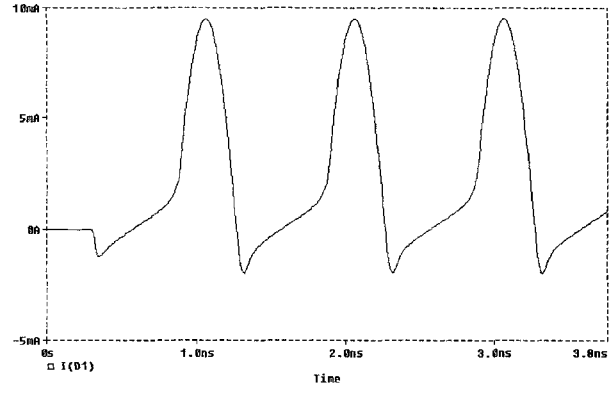


Fig. 4. SPICE simulation of the diode-terminated microstrip connection: current computed at the diode cell.

at a considerable distance from the actual solution, unless a very short time interval is assumed. This, in turn, may dramatically slow down the NR convergence, or even prevent the iterative loop from converging at all. Hence, if a constant time step is used throughout the simulation, its value must be settled to a conservative "*a priori*" estimate. Such an estimate can be worked out only by heuristic reasoning, and, in some circumstances, it may impose a much smaller time step than the one required by the Courant stability criterion. It is worth stressing how, within this scheme, any abrupt (and thus short) signal transition may actually impose a short time step to the whole simulation. From this point of view, it would be preferrable to reduce temporarily the time step only when required to ensure the convergence of the NR algorithm. To this purpose, let us now consider the plain FDTD algorithm in Table I.

According to the FDTD leapfrog algorithm, E- and H-field components are extracted from two separate sets of equations. Within each set, equations are completely independent of each other. The update of E- and H-field components can therefore be performed in an arbitrary order. In particular, equations pertaining to lumped-element cells can be isolated from their sets and preliminarily solved. This allows the convergence of the NR procedure to be checked in a relatively inexpensive

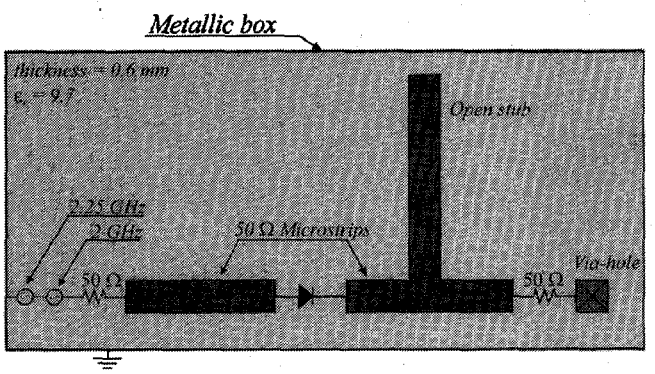
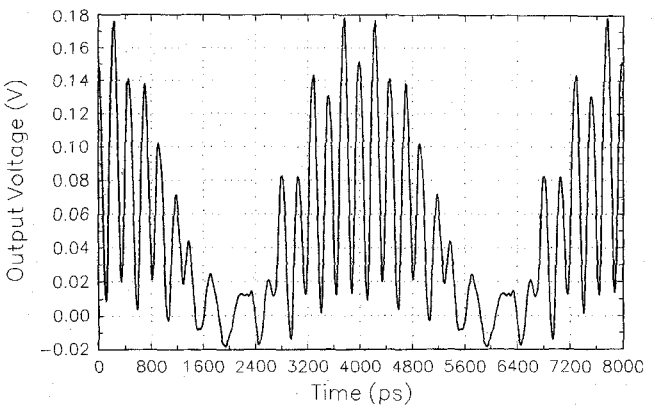
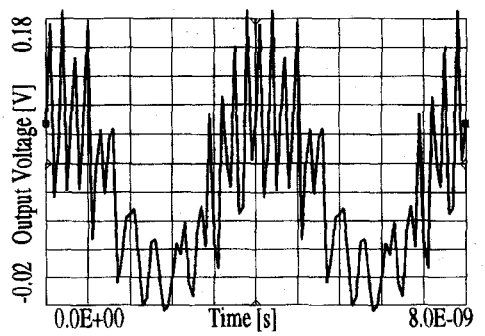


Fig. 5. Simulation of the unbalanced Schottky-diode mixer: circuit layout.



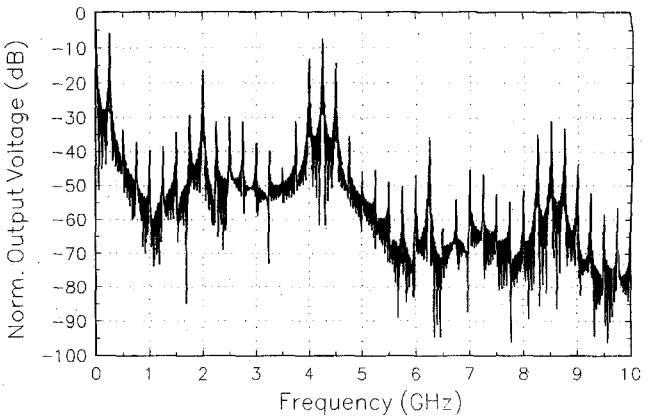
(a)



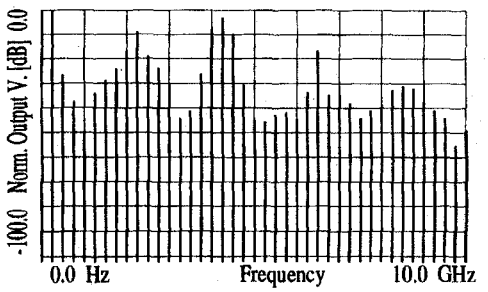
(b)

Fig. 6. Simulation of the unbalanced Schottky-diode mixer: comparison between time domain responses obtained from (a) FDTD simulation and (b) harmonic balance (HP-MDS). (Turn-on transients of voltage sources are not shown in figure.)

way. In fact, according to the scheme presented in Section II, lumped elements actually contribute to the set of E-field equations only, the convergence of which is therefore to be kept under control. In order to update any E-field component, fresh (i.e., consistent with the time step under check) updates of its neighboring H-field components are needed. The actual check, therefore, first locally solves for the H-field components close to the lumped-element cells then evaluates the convergence of the nonlinear E-field equations. Since only a few lumped elements are usually present (with respect to the overall number of field components), the computational overhead introduced by such a preliminary check is indeed almost negligible.



(a)



(b)

Fig. 7. Simulation of the unbalanced Schottky-diode mixer: comparison between frequency spectra obtained from (a) FDTD and (b) HP-MDS.

An adaptive scheme is thus devised in which the optimal time step (i.e., the largest one ensuring convergence) is selected at run time, prior to each field update. The resulting algorithm is summarized in Table II.

IV. Simulation Results

The first structure simulated consists of a simple clamping diode placed across a parallel-plate waveguide. The guide is 30 mm long, 3.7 mm wide, and 0.5 mm thick, this leading to a characteristic impedance of about 50 Ω. First-order absorbing boundary conditions [12] have been used to terminate the mesh far from the line boundaries. The mesh is uniformly spaced and counts 12 × 19 × 40 cells. The cross section of the dielectric layer between the plates is discretized with 2 × 4 cells. The input signal comes from a resistive voltage source [7] and consists of a 1-GHz sinusoid, smoothly switched on (at $t = 0$) by a Gaussian envelope. A pn diode is located at the opposite end of the line, connected across the plates. The diode current computed by FDTD simulation is shown in Fig. 3. Here, predictions of the ideal (dashed line) and nonideal (solid line) diode models are compared. The nonideal response significantly deviates from the ideal one, mainly due to the diode turn-off transient. A further comparison is given in Fig. 4, where SPICE simulation results for a similar structure are plotted. The simple case at hand easily lends itself to the modeling approach adopted by SPICE (more specifically, the ideal T-device model [13] has been used in this case), so that an excellent agreement between the two results is found.

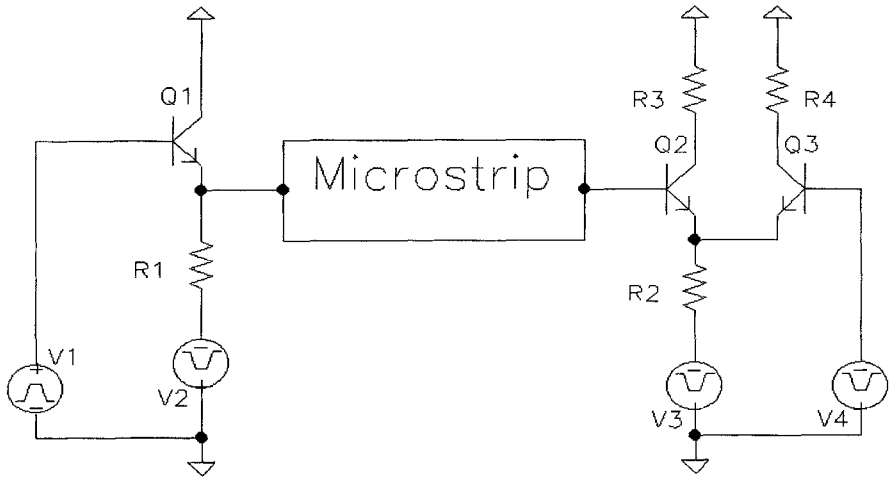


Fig. 8. ECL gate interconnection: schematic view of the simulated circuit.

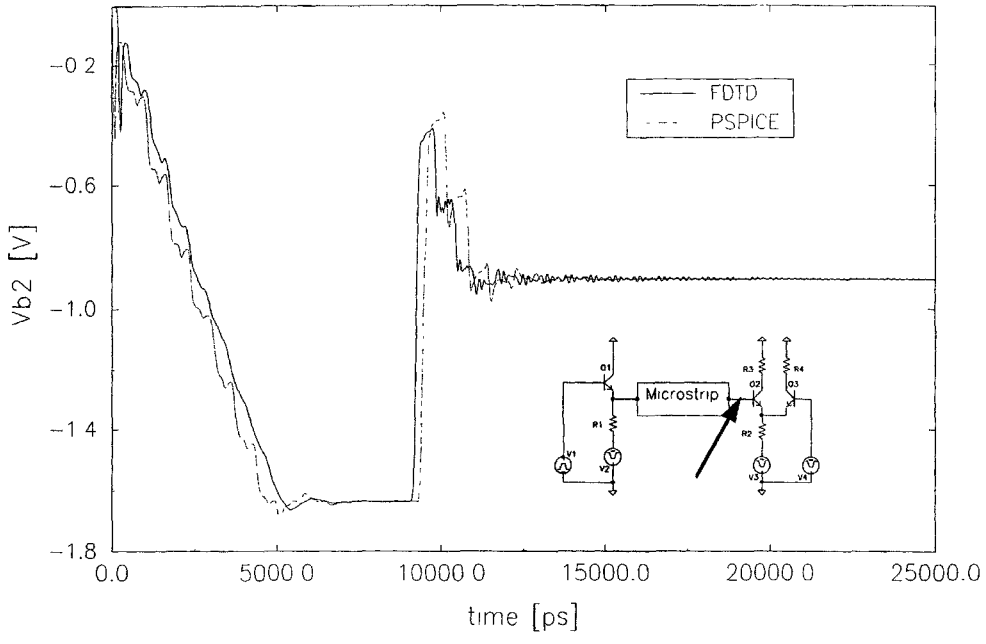


Fig. 9. ECL gate interconnection: input signal at the receiving gate (see inset).

A more realistic application is shown in Fig. 5 and consists of an unbalanced mixer based on a Schottky diode connected to a filtering microstrip stub. The line is terminated by a load resistor connected to the ground plane through a via-hole, while the simulation domain is bounded by the metallic package. Two resistive voltage sources are placed at the microstrip input and feed the line with two sinusoidal signals (2 and 2.25 GHz). A 47 × 46 × 107 graded (i.e., nonuniform) mesh [14] has been used to increase the cell density close to the field singularities. The diode is actually placed across a single cell and the remaining width of the microstrip gap is filled with a line of lumped resistors. This allows for a careful description of the electromagnetic behavior of the microstrip gap (seven cells are actually employed in this example), whereas the series resistors may account for the ohmic behavior of the diode neutral regions and of the connections.

The transient response of the FDTD simulation is shown in Fig. 6(a), while the extracted frequency spectrum is shown in Fig. 7(a). Such results are in fair agreement with the corresponding results of Figs. 6(b) and 7(b), respectively, predicted by HP-MDS [15] through the harmonic balance technique. Small, quantitative discrepancies between Figs. 6 and 7 are to be ascribed to the different models adopted for the passive network. In particular, the full-wave technique exploited by FDTD accounts for a more comprehensive physical picture of the structure in Fig. 5.

In order to illustrate the variable time-step algorithm features, a more complicated example has been conceived. As shown in Fig. 8, it consists of a microstrip transmission line connecting two logic gates. More specifically, the emitter follower on the left represents the output stage of an ECL-technology NOR gate, whereas the differential pair on the

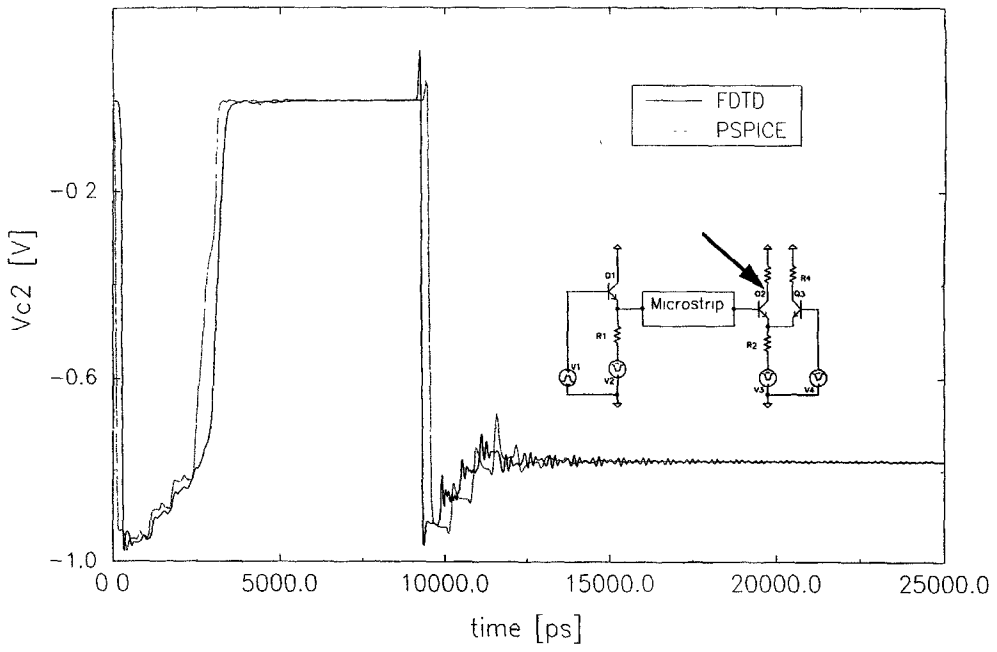


Fig. 10. ECL gate interconnection: output signal at the input stage of the receiving gate (see inset).

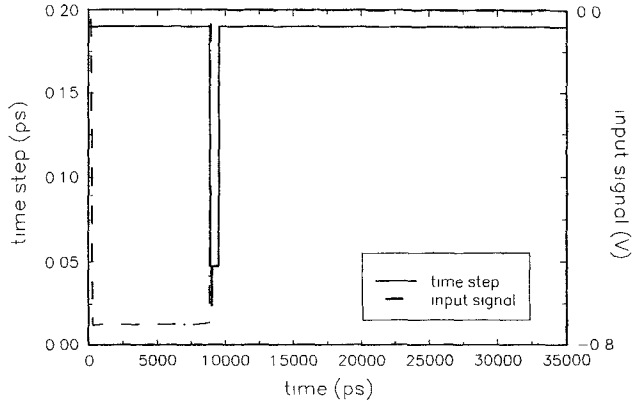


Fig. 11. ECL gate interconnection: adaptive adjustment of the simulation time step.

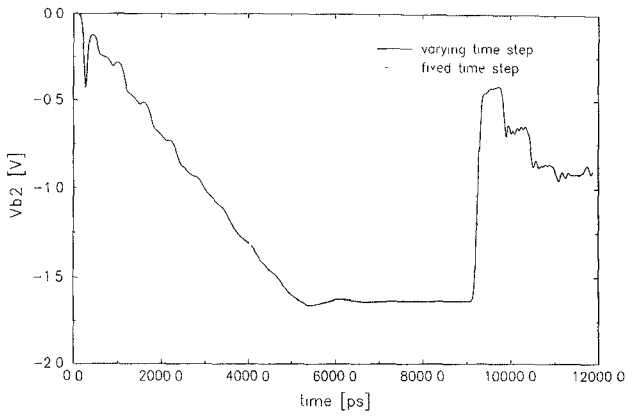


Fig. 12. ECL gate interconnection: input signal at the receiving gate, as computed with the time adaptive scheme (solid line) and the fixed time step scheme (dashed line).

right stands for the input stage of an identical gate. A 35-mm-long, 0.8-mm-wide microstrip (the characteristic impedance of which is thus equal to 42 Ω) drives the signal between the two gates.

A graded mesh, consisting of 15 × 21 × 100 cells, has been used in this case, too. The edge size ranges from 0.1 to 1 mm; in particular, the grid has been refined close to discontinuities and lumped elements, as well as across the dielectric layer. The presence of fringing fields at the microstrip edges has been accounted for by extending the simulation domain slightly beyond the edges themselves. The simulation aims at evaluating the influence of line mismatchings on the signal propagation. The digital signal along the microstrip is first settled to its low value; to this purpose, power supplies V_2, V_3, V_4 in Fig. 8, as well as the signal source V_1, are brought to their regime values through Gaussian voltage ramps. After such a regime has been attained, the input signal switches to its high value, that is, a voltage step ($\Delta V = 0.75$ V, $T_{\text{rise}} = 100$ ps) is applied to the base of Q_1. Fig. 9 shows the simulated response of the circuit, probed at the input of the receiving gate. Due to reflections at both ends of the line, the signal comes to its steady-state value following a "staircase" pattern, which results from the superposition of several signal components bouncing back and forth along the microstrip [16]. Fig. 10 refers to the inverting output of the differential pair and shows how, due to the saturation of the input-stage transfer characteristic, the signal overshoot is attenuated so that the degraded signal is, to some extent, regenerated. Again, computed results well compare with SPICE outputs, thus providing validation of the method.

Due to the nature of the input signal, which alternates steep ramps to quiescent states, the present example represents a challenging test for the transient-simulation strategy introduced in Section III. The performance of the adaptive algorithm is illustrated by Fig. 11. During most of the simulation, the time step is kept at its upper bound (actually settled by the Courant criterion); however, as the input voltage abruptly

changes, the time step is automatically reduced by almost an order of magnitude to allow for NR iterative loop convergence. As soon as a milder behavior of the signals is recovered, the time step relaxes back to its original value. The net CPU-time saving has been evaluated by imposing a constant time step to the same simulation. Such a time step has been fixed at the minimum value required by the above adaption. It therefore consists of an optimally tailored figure; without the hint coming from the adaptive algorithm, a more conservative value (i.e., a shorter time step) should have been selected. The almost identical responses of the two simulations are compared in Fig. 12, thus demonstrating the reliability of the adaptive algorithm. The CPU times required (on a HP 735 workstation) by the conventional and by the time adaptive simulations were 17h 20′ and 3h 58′, respectively. A 4.4 performance ratio is thus obtained. Such a figure is actually slightly worse than the average time step ratio, due to the computational cost of the convergence check described in previous section.

V. Conclusion

A mixed-mode circuit simulator has been developed, based on the lumped-element FDTD technique. Special care has been devoted to make it suitable for the efficient simulation of realistic circuits. In particular, the dynamic behavior of bipolar devices has been taken into account by incorporating models of the nonlinear junction and diffusion capacitances. Equations of such models have been discretized consistently with the leapfrog algorithm adopted for the solution of Maxwell's equations.

The code is thus capable of simulating lumped BJT's, pn and Schottky junction diodes. Lumped resistors, capacitors, and inductors, as well as independent (nonideal) voltage sources, are also available. These elements, in turn, can be regarded as elementary building blocks, suitable for assembling large-signal models of further elements.

The efficiency of the lumped-element FDTD algorithm has been enhanced by implementing a variable time step, adaptively adjusted during the simulation. Such a run-time optimization: 1) allows for substantial savings of computational resources; and 2) makes the scheme more robust. The time step adaption, in fact, prevents the iterative solution algorithm from crashing because of the poor quality of the initial guess.

We believe the present combination of comprehensive device models and efficient solution techniques makes the code a reliable tool for the accurate simulation of high-frequency analog and digital circuits. This has been demonstrated by some simulation examples, including a nonlinear microwave circuit and a subset of a high-speed digital board. Comparison with results coming from more conventional analysis tools have been carried out: although computational efforts are still not comparable, an excellent agreement between simulation results is found in all cases. To this regard, it should be emphasized that the above examples have been purposely conceived to validate the method. Actually, the application range of the lumped-elements FDTD algorithm is perspectively much wider and includes a number of increasingly important effects (e.g., radiative effects, crosstalk, line discontinuities, package interactions) which can hardly be taken into account by most existing circuit analysis programs.

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Paolo Ciampolini (M'91) graduated *cum laude* in electronic engineering from the University of Bologna, Bologna, Italy. In 1989, he received the Ph.D. degree in electronics and computer sciences from the University of Bologna.

From 1983 to 1992, he was with the Dipartimento di Elettronica, Informatica e Sistemistica (DEIS) University of Bologna, then in the same year became a Research and Teaching Assistant. In 1992, he was appointed Associate Professor of Electronics at the University of Perugia, Perugia, Italy. His research interests are mainly in the field of technology CAD tools. At present, he is engaged in activities related to three-dimensional simulation of semiconductor devices, advanced models for device simulation, and modeling of integrated microsensors and high-frequency devices and circuits.

Paolo Mezzanotte was born in Perugia, Italy, in 1965. He received the Laurea degree in electronic engineering from the University of Ancona in 1991 with a thesis on FDTD analysis of GTEM cell.

Since 1992, he has been working on FDTD analysis of microwave structures in cooperation with the Institute of Electronics of the University of Perugia, where in 1993 he entered the Ph.D. program in electronic engineering. His main field of interest is the application of numerical methods to the study of components and structures for microwave and millimeter-wave circuits.

Luca Roselli (M'92) was born in Firenze, Italy, in 1962. He received the Laurea degree in electrical engineering from the University of Firenze in 1988.

From 1988 to 1991, he worked at the University of Firenze on SAW devices. In November 1991, he joined the Institute of Electronics, University of Perugia, Perugia, Italy, as a Research Assistant. Since 1994 he has taught the "Electronic Devices" course at the same University. Since 1995 he has been a reviewer for the IEEE MICROWAVE AND GUIDED WAVE LETTERS. His research interests include the design and development of millimeter-wave and microwave active and passive circuits by numerical techniques.

Roberto Sorrentino (M'74–SM'84–F'90) received the Doctor degree in electronic engineering from the University of Rome "La Sapienza," Rome, Italy, in 1971.

In 1971, he joined the Department of Electronics, University of Rome "La Sapienza," where he became an Assistant Professor of Microwaves in 1974. He was also Professore Incaricato, University of Catania, in 1975 and 1976, at the University of Ancona in 1976 and 1977, and at the University of Rome "La Sapienza", from 1977 to 1982, where he was an Associate Professor from 1982 to 1986. In 1983 and 1986, he was appointed as a Research Fellow at the University of Texas at Austin. From 1986 to 1990, he was a Professor at the Second University of Rome "Tor Vergata." Since November 1990, he has been a Professor, University of Perugia, Perugia, Italy, where he was the Chairman of the Electronic Institute, Director of the Computing Center, and is presently the Dean of the Faculty of Engineering. His research activities have been concerned with electromagnetic wave propagation in anisotropic media, interaction of electromagnetic fields with biological tissues, mainly with the analysis and design of microwave and millimeter-wave passive circuits. He has contributed to the planar-circuit approach for the analysis of microstrip circuits and to the development of numerical techniques for the modeling of components in planar and quasi-planar configurations.

Dr. Sorrentino is the Editor-in-Chief of the IEEE MICROWAVE AND GUIDED WAVE LETTERS, a member of the editorial boards of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the *International Journal on Numerical Modelling*, and the *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*.